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| Serial No: |
| **Final Examination** |
| **Total Time: 3 Hour** |
| **Total Marks: 95** |
| \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  Signature of Invigilator |

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| **EE-227 Digital**  **Logic Design** |
| Monday, August 6, 2018 |
| **Course Instructor** |
| Dr. Mehwish Hassan |

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| **\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**  Student Name Roll No Section Student Signature |
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## DO NOT OPEN THE QUESTION BOOK OR START UNTIL INSTRUCTED.

**Instructions:**

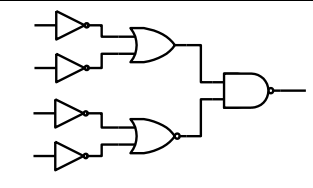
1. Attempt on question paper. Attempt all of them. Read the question carefully, understand the question, and then attempt it.
2. No additional sheet will be provided for rough work. Use and mark the back of the last page for rough work.
3. Write in the space provided for each question/part and if you need more space write on the back side of the paper and clearly mark question and part number etc.
4. After asked to commence the exam, please verify that you have **(17)** different printed pages including this title page. There are total of **9 questions**.
5. **Calculator is NOT allowed.**
6. Use permanent ink pens only. Any part done using soft pencil will not be marked and cannot be claimed for rechecking.
7. **For each question show your complete method in solution**.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Questions** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **Total** |
| **Total**  **Marks** | **10** | **10** | **10** | **10** | **10** | **10** | **15** | **10** | **10** | **95** |
| **Marks Obtained** |  |  |  |  |  |  |  |  |  |  |

**Vetted By: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_Vetter Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

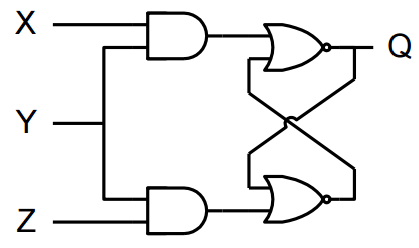
**Question No.1 [10]**

1. F = (A’B’+CD) E’. Its complement is:
   1. (A’+B’)(C+D)+E’
   2. (A+B)(C’D’)+E
   3. (AB)(C’D’)+E
   4. (A+B)(C’+D’)+E
2. Given F1 (A,B,C,D) = Σ ( 0, 2, 4, 8 ), F2 (A,B,C,D) = Σ ( 1, 2, 3, 4, 15 ) and F3 = F1 + F2 then:
   1. F3 (A,B,C,D) = Σ ( 2, 4 )
   2. F3 (A,B,C,D) = Σ ( 0, 1, 2, 3, 4, 8 )
   3. F3 (A,B,C,D) = Σ ( 0, 1, 2, 3, 4, 8, 15 )
   4. F3 (A,B,C,D) = Σ ( 5, 6, 7, 9, 10, 11, 12, 13, 14 )
3. The shown circuit can be implemented using a minimum of



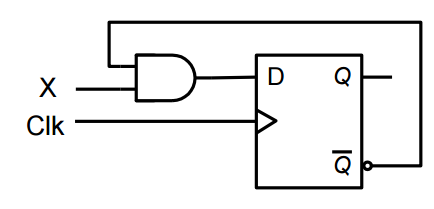
* 1. 3 NAND gates
  2. 4 NAND gates
  3. 4 NAND and 1 NOR gates
  4. 4 NAND and 2 NOR gates

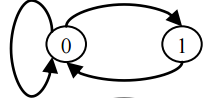
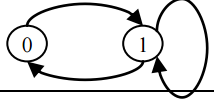
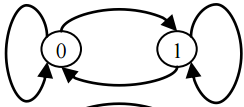
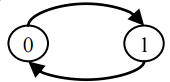
1. To “set” the shown latch, we should apply:



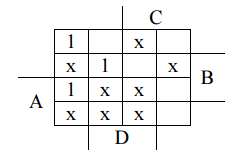
* 1. X = 1, Y = 0 and Z = 0
  2. X = 1, Y = 1 and Z = 0
  3. X = 0, Y = 1 and Z = 0
  4. X = 0, Y = 1 and Z = 1

1. The correct state diagram for the shown circuit is:



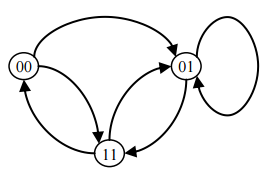
* 1. 
  2. 
  3. 
  4. 

1. To implement the Boolean function F = A ⊕ B ⊕ C we can use a 3-to-8 decoder and connect:
   1. 3 different lines from its output to an OR gate
   2. 4 different lines from its output to an OR gate
   3. 5 different lines from its output to an OR gate
   4. 6 different lines from its output to an OR gate
2. For the shown K-map, the simplified Boolean expression F(A,B,C,D):



* 1. 2 groups, each consisting of 4 squares
  2. 3 groups, each consisting of 4 squares
  3. 4 groups, each consisting of 4 squares
  4. 2 groups of 4 squares and 1 group of 2 squares

1. The Boolean expression (A+B+C) (A’+B’+C’) has a dual which is:
   1. (A’+B’+C’) (A+B+C)
   2. (A’+B’+C’) + (A+B+C)
   3. (A B C) (A’ B’ C’)
   4. (A B C) + (A’ B’ C’)
2. Two T Flip-Flops, A and B, are used to implement the shown state diagram. To go from state AB = 01 to AB = 11 we need:



* 1. TA = 0, TB = 1
  2. TA = 1, TB = 0
  3. TA = 1, TB = 1
  4. TA = 1, TB = x (x is don’t care)

1. For the function F(w,x,y,z) = w’y + y’z+ wxz +w’y’z’ + xyz’, the essential prime implicants are:
   1. w’y, y’z, w’y’z’, xyz’
   2. w’y, y’z, wxz
   3. wx’y, z, w’
   4. wx’y, z, w’

**Question No.2 [10]**

Draw and label the circuit diagram of a universal shift register using four 4 x 1 multiplexers and four D flip flops. The shift register should operate according to the following table.

|  |  |  |
| --- | --- | --- |
| S1 | S0 | Operation |
| 0 | 0 | Complement inputs |
| 0 | 1 | Shift right |
| 1 | 0 | Hold Value |
| 1 | 1 | Shift left |

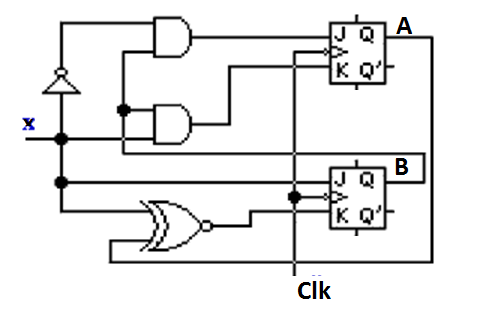
**Question No.3 [10]**

Design a sequential circuit for following State transition diagram using JK flip-flop. This circuit has three flip flops A, B, C; one input x and one output y. Treat unused states as don’t cares.



**Question No.4 [10]**

Analyze the following circuit with JK flip flops and provide the flip flop input equations, state table and state diagram.



**Question No.5 [10]**

Design the smallest possible circuit of a controlled 3 – bit counter (Control input C) using D Flip-Flops

When input C=0 the counter counts up even numbers: 000 → 010 → 100 → 110 → 000 → etc.

When input C=1 the counter counts down odd numbers: 000− → 111 → 101 → 011 → 001 → 000

Provide:

1. State diagram
2. State table
3. Expressions for inputs of D Flip-Flops
4. Circuit Diagram

**Question No.6 [6 + 4 = 10]**

1. Draw the circuits of SR Latch with NAND and NOR gates. Write function table for each.
2. Draw and label the circuit diagram of a positive edge triggered D-flip flop in master slave configuration using two D latch blocks.

**Question No.7 [10+ 5 = 15]**

1. Design a 4-bit priority encoder with following priority sequence.

**D2 < D0 < D3 < D1**

1. A majority function F takes three 1-bit inputs a,b and c, and produces a single bit as output that is one if and only if two or more bits of the input are one. Design this circuit using an 8:1 multiplexor.

**Question No.8 [10]**

Implement the following functions using the PAL. Draw PAL diagram. NOTE: Functions are treated as simplified.

W(A,B,C,D) = ABC’ +B’CD’

X (A,B,C,D) = A + BD

Y(A,B,C,D) = ABC’ + B’CD’ + AC’D’ + A’B’C’D

Z (A,B,C,D) = A’B + CD + B’D’

**Question No.9 [10]**

Implement following functions using 16 X 4 ROM. Give the ROM table and Draw the circuit.

F1 (A,B,C,D) = A' C' + B' D' + ABC

F2 (A,B,C,D) = B' C + ACD + A' B C'

F3 (A,B,C,D) = C' D' + CD + A' BC + AC' D'

F4 (A,B,C,D) = BC' + BCD' + ABC

**Rough Work**